In the Claims:

1. (Currently Amended) An integrated circuit device, comprising:

a data inversion circuit that is configured to evaluate bit differences between first and second ordered groups of data received in parallel at inputs thereof by performing bit-to-bit comparisons between corresponding bits in the first and second ordered groups of data and is further configured to generate versions of the first and second ordered groups of data in parallel at outputs thereof, wherein the version of the second ordered group of data is an inverted version of the second ordered group of data when a number of bit differences between the version of the first ordered group of data and the second ordered group of data is greater than one-half the number of bits of data within the second ordered group of data, said data inversion circuit comprising an XOR circuit that is configured to receive the first and second ordered groups of data, a comparator that is configured to generate a first internal parity signal in response to signals generated by said XOR circuit and a parity signal generator that is configured to generate a second external parity signal in response to a first external parity signal and the first internal parity signal ~~signal~~.

2. (Original) The device of Claim 1, wherein the first external parity signal identifies whether the version of the first ordered group of data is an inverted or noninverted version of the first ordered group of data and the second external parity signal identifies whether the version of the second ordered group of data is an inverted or noninverted version of the second ordered group of data.

3. (Currently Amended) The device of Claim 1, wherein said comparator is configured to generate a pair of complementary internal parity signals in response to signals generated by said ~~first~~ XOR circuit.

4. (Original) The device of Claim 1, wherein said parity signal generator is configured to generate a pair of complementary internal parity signals in response to the first internal parity signal.

5. (Previously Presented) The device of Claim 3, wherein said parity signal generator is configured to select a first one of the pair of complementary internal parity signals as the second external parity signal when the first external parity signal is in a first logic state and is further configured to select a second one of the pair of complementary internal parity signals as the second external parity signal when the first external parity signal is in a second logic state opposite the first logic state.

6. (Original) An integrated circuit device, comprising:

a data inversion circuit that is configured to evaluate bit differences between first and second ordered groups of data received in parallel at inputs thereof by performing bit-to-bit comparisons between corresponding bits in the first and second ordered groups of data and is further configured to generate a version of the first ordered group of data in parallel with an inverted version of the second ordered group of data at outputs thereof when a number of bit differences between the version of the first ordered group of data and the second ordered group of data is greater than one-half the number of bits of data within the second ordered group of data, said data inversion circuit comprising a plurality of parity signal generators that are configured to generate at least a first external parity signal that identifies whether the version of the first ordered group of data is an inverted or noninverted version of the first ordered group of data.

7. (Previously Presented) The device of Claim 6, wherein said data inversion circuit comprises at least one delay circuit that is configured to generate a delayed version of the first ordered group of data in response to the first ordered group of data and is further configured to generate the version of the first ordered group of data at an output of said data inversion circuit in response to the delayed version of the first ordered group of data and the first external parity signal.

8. (Currently Amended) The device of Claim 7, wherein a delay provided by ~~the~~ at least one delay circuit is of sufficient duration to maintain a delay margin between a leading edge of ~~the~~ at least a first external parity signal and corresponding leading edges of the data in the delayed version of the first ordered group of data, within a threshold delay margin.

9.-33. (Canceled)